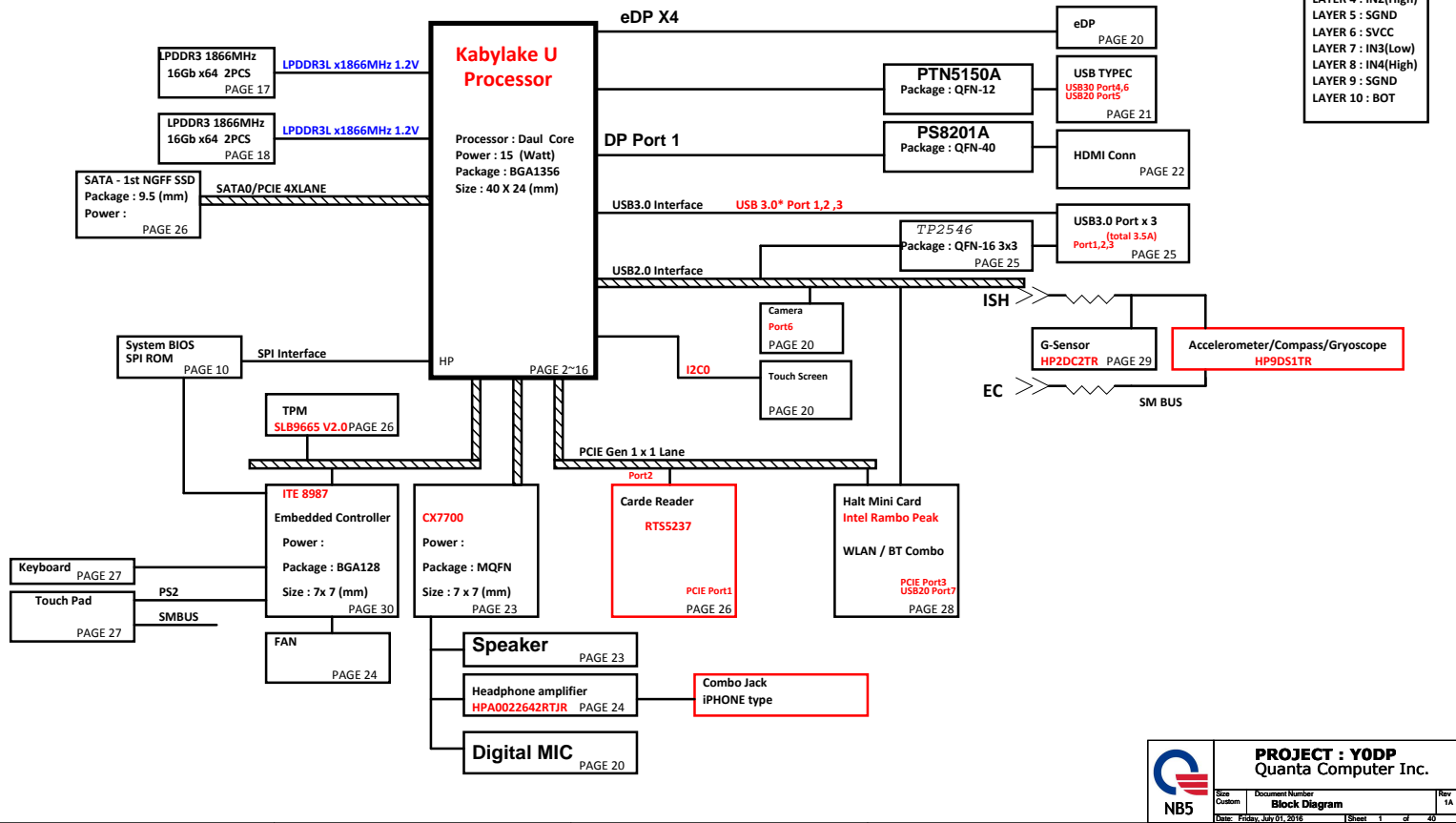


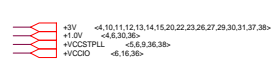
Pavlova Intel KABYLAKE ULT Platform Block Diagram

PCB 10L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(High)
 LAYER 5 : SGND
 LAYER 6 : SVCC
 LAYER 7 : IN3(Low)
 LAYER 8 : IN4(High)
 LAYER 9 : SGND
 LAYER 10 : BOT



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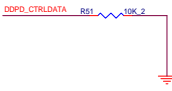


HDMI

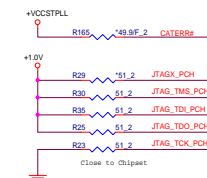
DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.



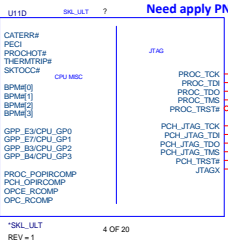
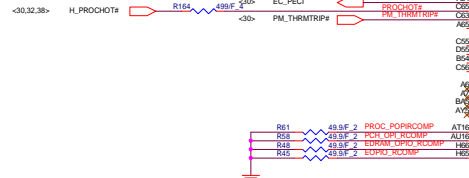
This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.



eDP_COMPID and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

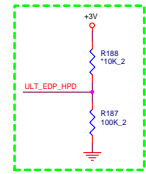


Close to Chipset



*SKL_ULT
REV = 1
4 OF 20

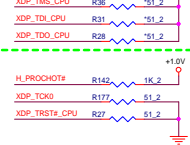
Reserve EDP_HPD opposites circuit!



Close to EC

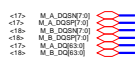


PLACE NEAR CPU



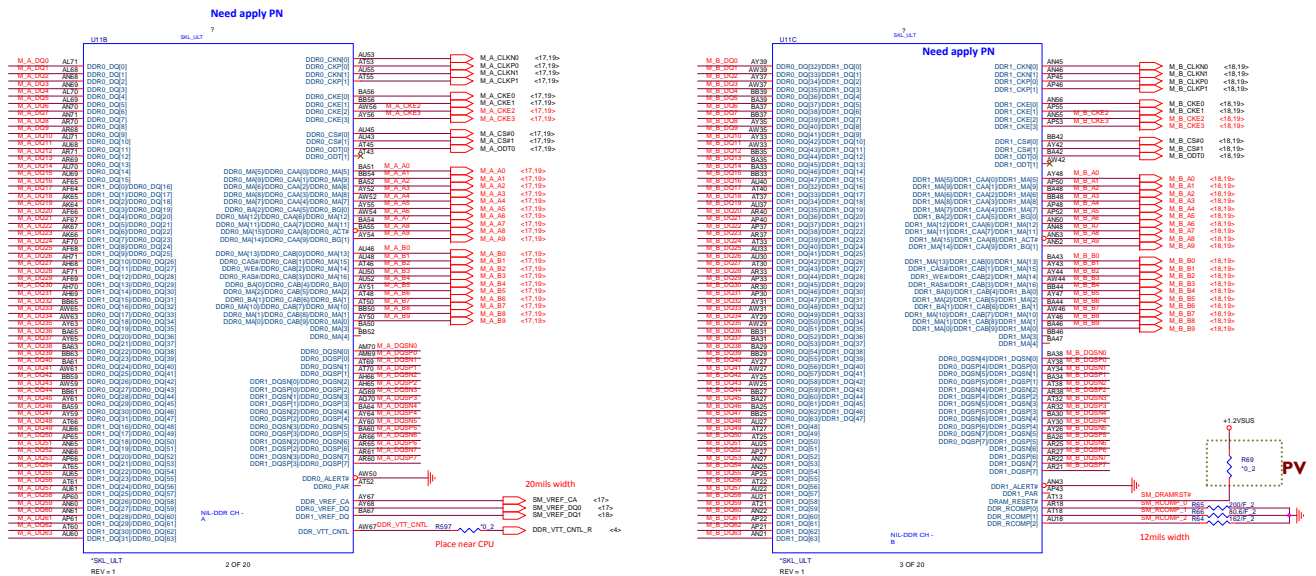
	PROJECT : YODP Quanta Computer Inc.		
	Set Custom	Document Number KBLU (1/14)	Rev 1A
	Date: Friday, July 01, 2016	Sheet 2 of 40	


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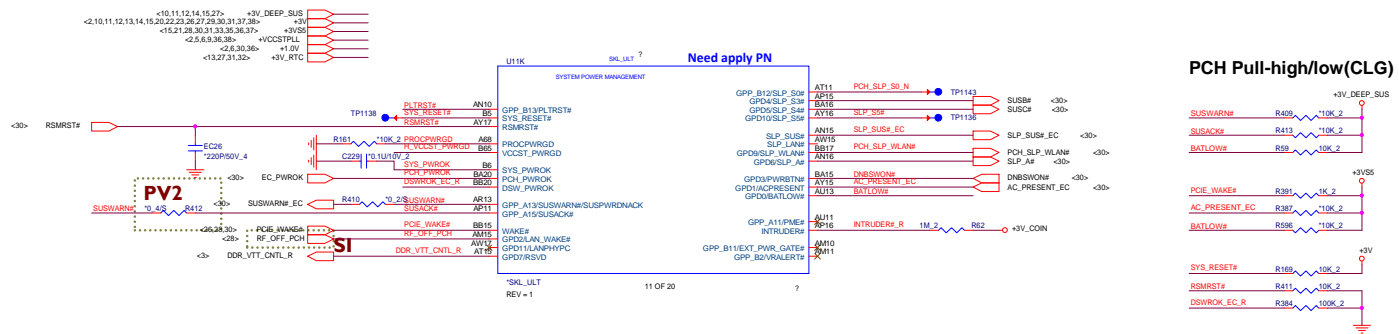


SkyLake ULT Processor (DDR3L)

 +1.2VSUS <6,17,18,22,34,36>



 NB5	PROJECT : YODP Quanta Computer Inc.		
	Title Custom	Document Number KBL U (2/14)	Rev 1A
Date: Friday, July 01, 2016		Sheet 3 of 40	

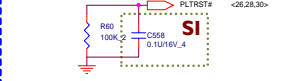


For DS3 Sequence

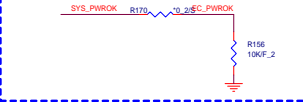


PLTRST#(CLG)

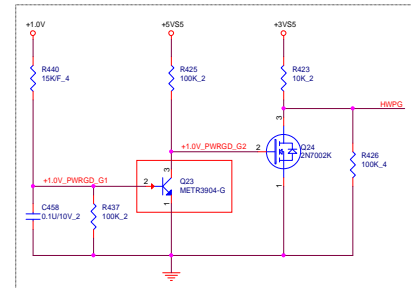
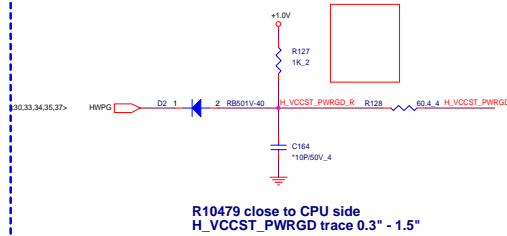
Check Q2010 Rise/Fall time less than 100ns



System PWR_OK(CLG)



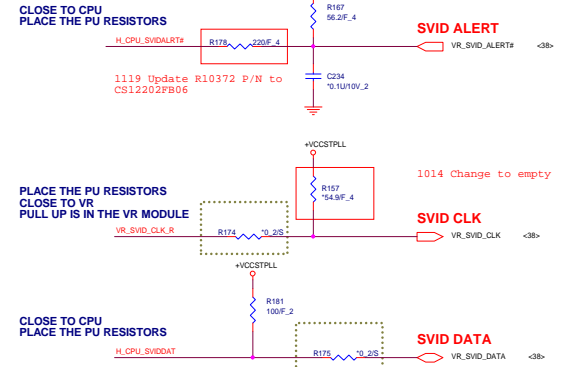
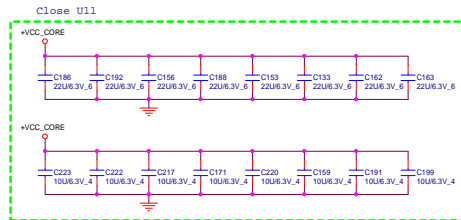
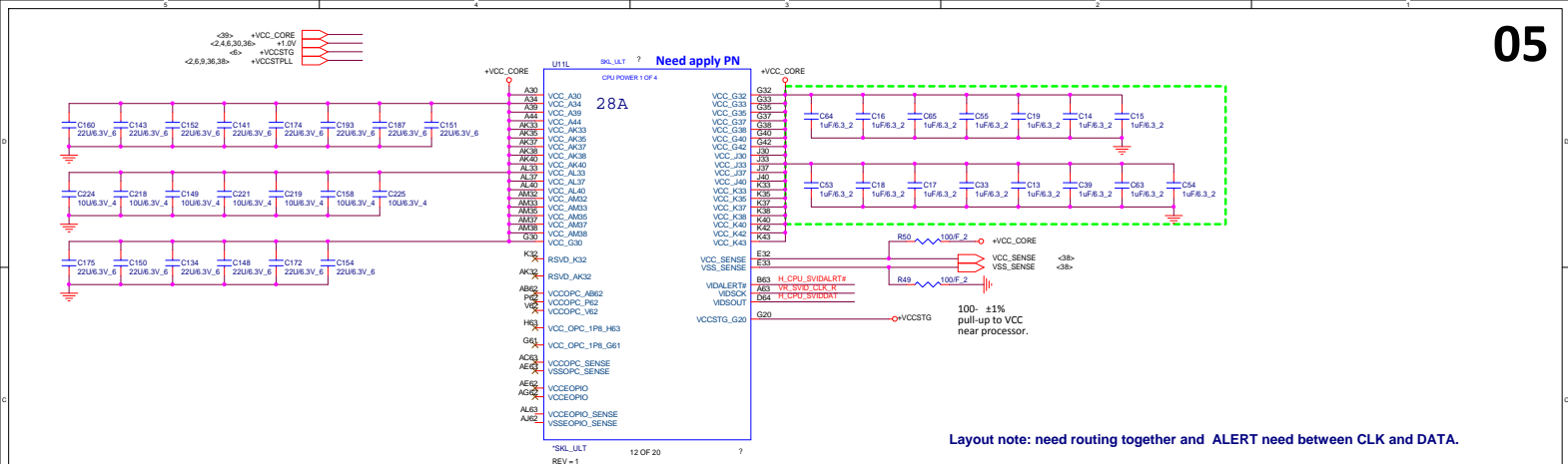
1211 Del
+VCCSTPPLL and R134



1110 Add Circuit for +1.0V Power Good

1118 Change Change Q7062 P/N from BA051440000 to BA039040020, Del D7002, D7003, R10526, R10527

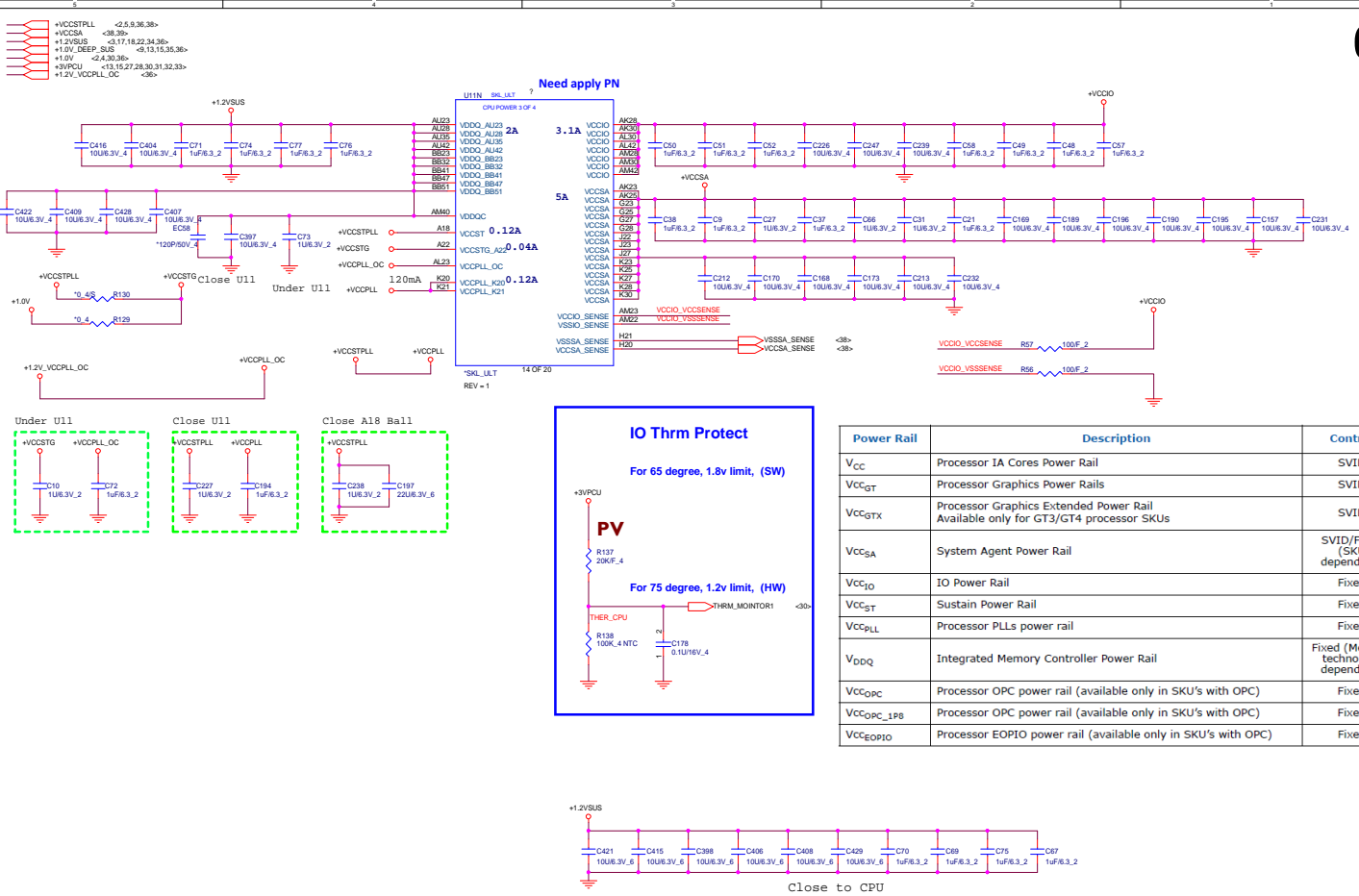
	PROJECT : YODP Quanta Computer Inc.		
	Doc Number	Doc Number	Rev 1A
	Doc Date	Doc Date	Doc Date

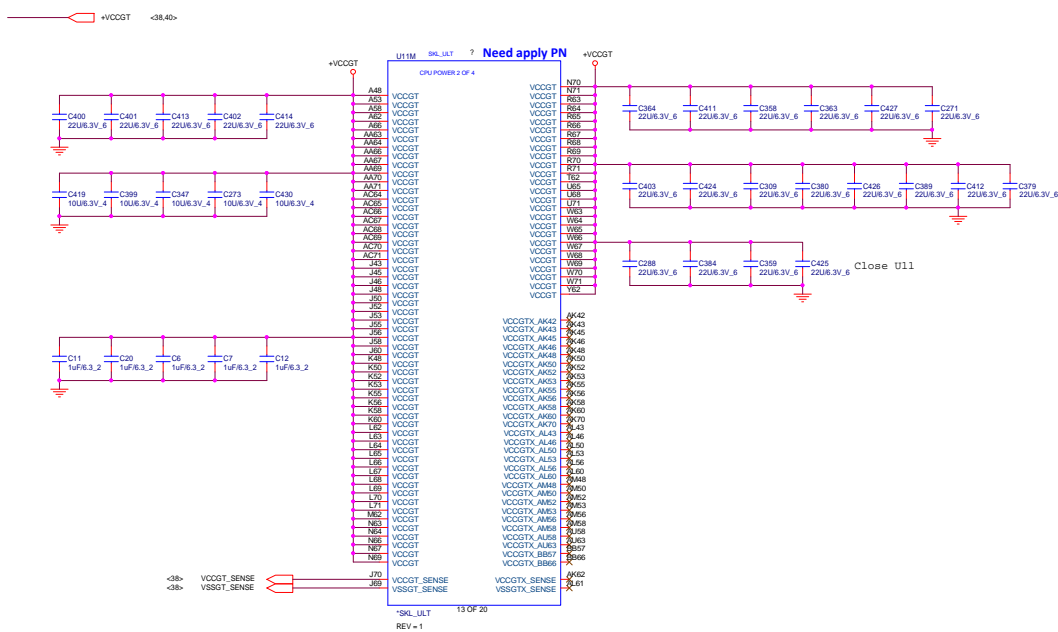


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CC} _{GT}	Processor Graphics Power Rails	SVID
V _{CC} _{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CC} _{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CC} _{IO}	IO Power Rail	Fixed
V _{CC} _{ST}	Sustain Power Rail	Fixed
V _{CC} _{PLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CC} _{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CC} _{OPC_1PB}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CC} _{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

PROJECT : YODP Quanta Computer Inc.		Rev 1A
NB5	Document Number KBL U (4/14)	Rev 1A
Drawn: Jody, July 01, 2018	Sheet 6 of 40	

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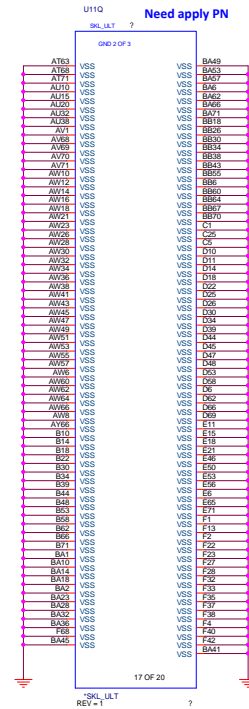
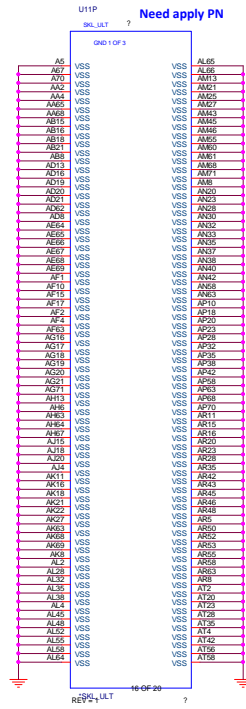
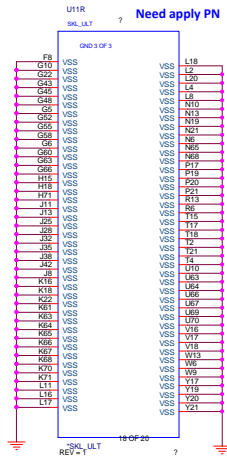


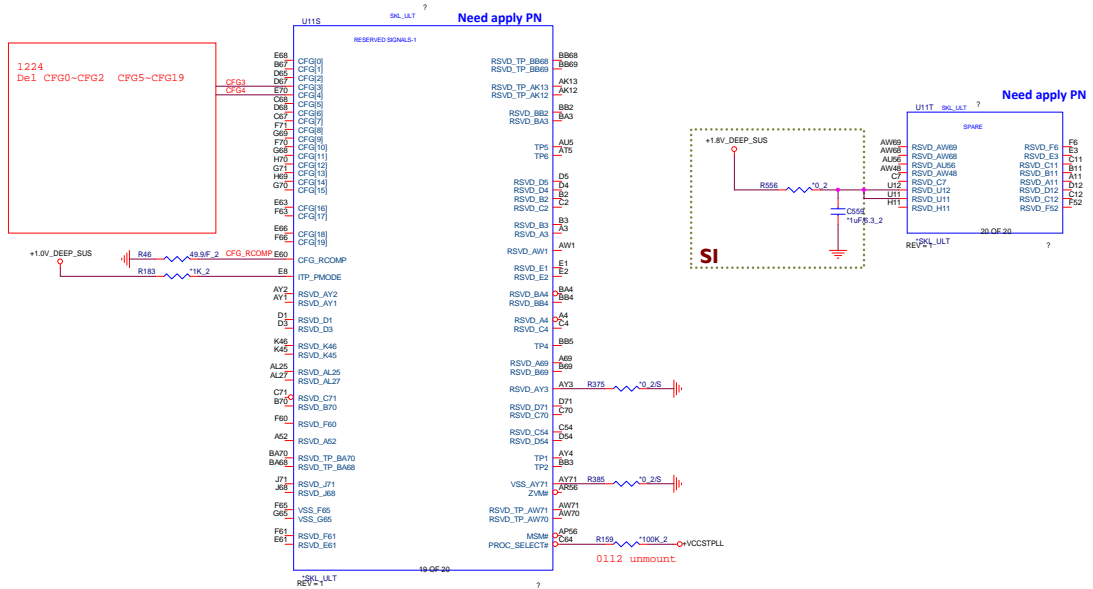


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1PB}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

			PROJECT : YODP Quanta Computer Inc.		
Set	Document Number	Rev	Set	Document Number	Rev
Current	KBL U (6/14)	1A	Current	KBL U (6/14)	1A
Date: Friday, July 01, 2016	Sheet 7 of 40		Date: Friday, July 01, 2016	Sheet 7 of 40	

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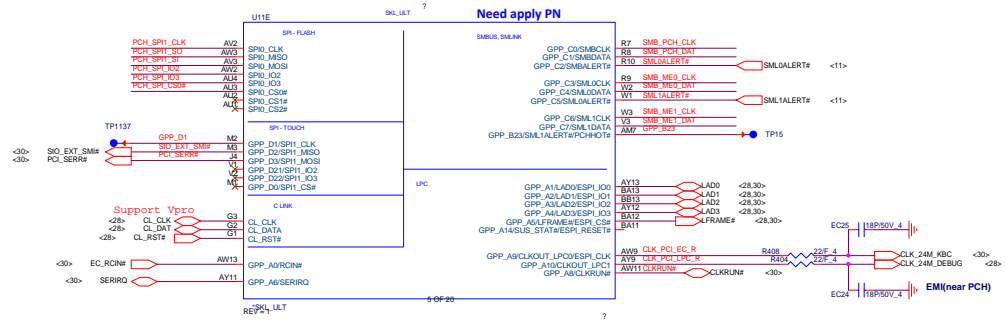




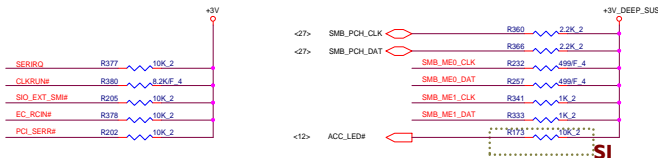
Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable)	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable: No physical DP attached to eDP	Enable: An ext DP device is connected to eDP	

+3V_DEEP_SUS <4,11,12,14,15,27>
 +3V <2,4,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38>
 +5V <22,23,24,27,37>
 +1.0V <2,4,6,30,36>
 +3V55 <4,15,21,28,30,31,33,35,36,37>



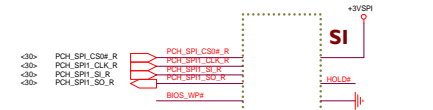
GPIO Pull UP



PCH SPI ROM(CLG)

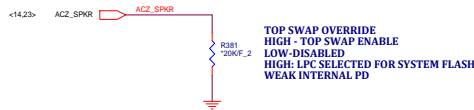
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket

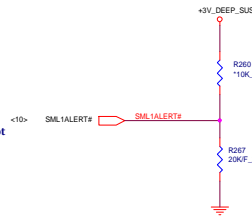
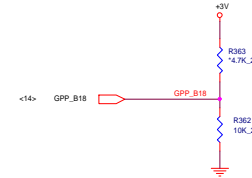
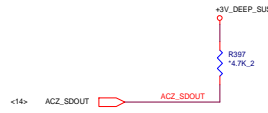
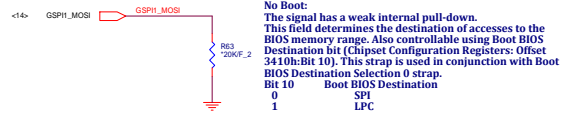
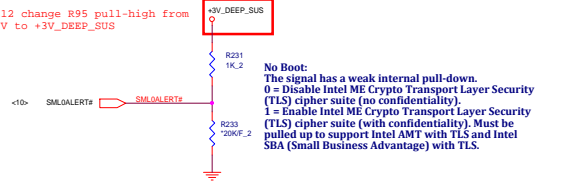



Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



1212 change R95 pull-high from
+3V to +3V_DEEP_SUS



	PROJECT : YODP Quanta Computer Inc.		
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PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	CardReader	Port0	Un-used
Port2	Un-used	Port1	CardReader
Port3	WLAN	Port2	WLAN
Port4	Un-used	Port3	Un-used
Port5	SSD	Port4	Un-used
Port6	SSD	Port5	SSD
Port7	SSD		
Port8	SSD		
Port9	Un-used		
Port10	Un-used		

USB3.0 Port Mapping Table

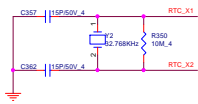
USB3.0	Function
PORT-1	USB3.0 MB-2
PORT-2	USB3.0 MB-3
PORT-3	USB3.0 MB-4
PORT-4,6	TYPE C

USB2.0 Port Mapping Table

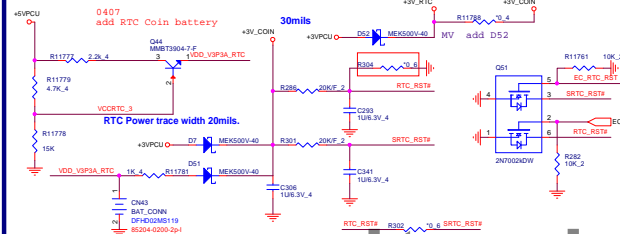
USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	NC
PORT-5	TYPE C
PORT-6	Camera
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

	PROJECT : YODP Quanta Computer Inc.		Rev 1A	
	Doc KBL U (11/14)	Date Friday, July 01, 2016		Sheet 12 of 40

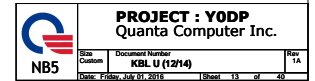
www.aitech1.ru



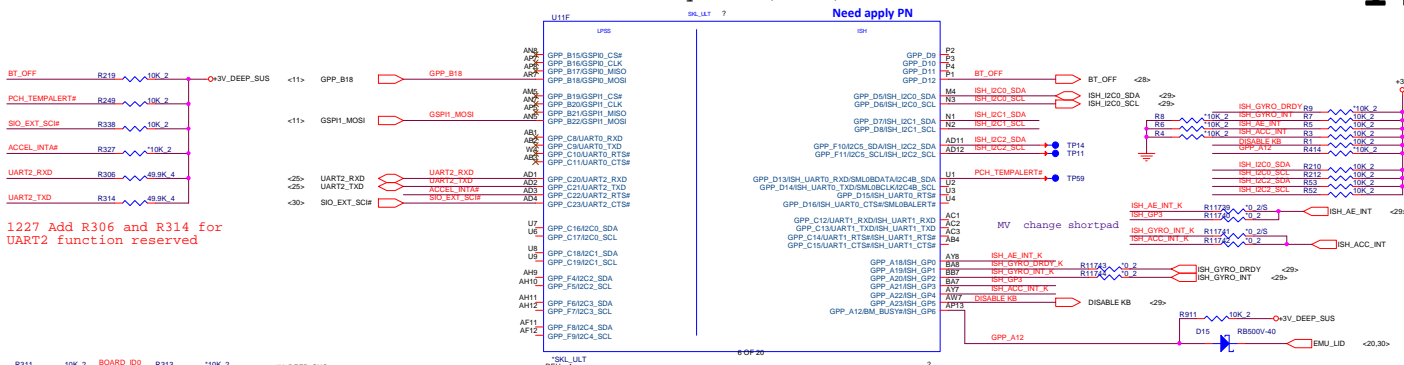
 +3V_RTC <27,31,32>
+3VPCU <6,15,27,28,30,31,32,33>



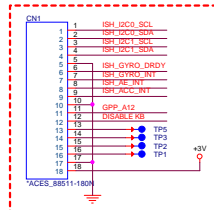
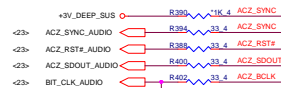
The schematic diagram illustrates the XTAL24 circuit. It features a 24MHz ±30PPM crystal (Y1) connected to a 1M4 resistor (R176) and two 27pF capacitors (C207 and C208). The circuit is powered by TPS50 and TPS1, with XTAL24_IN and XTAL24_OUT signals.



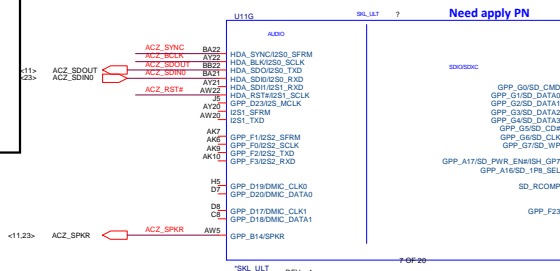
Skylake (GPIO)

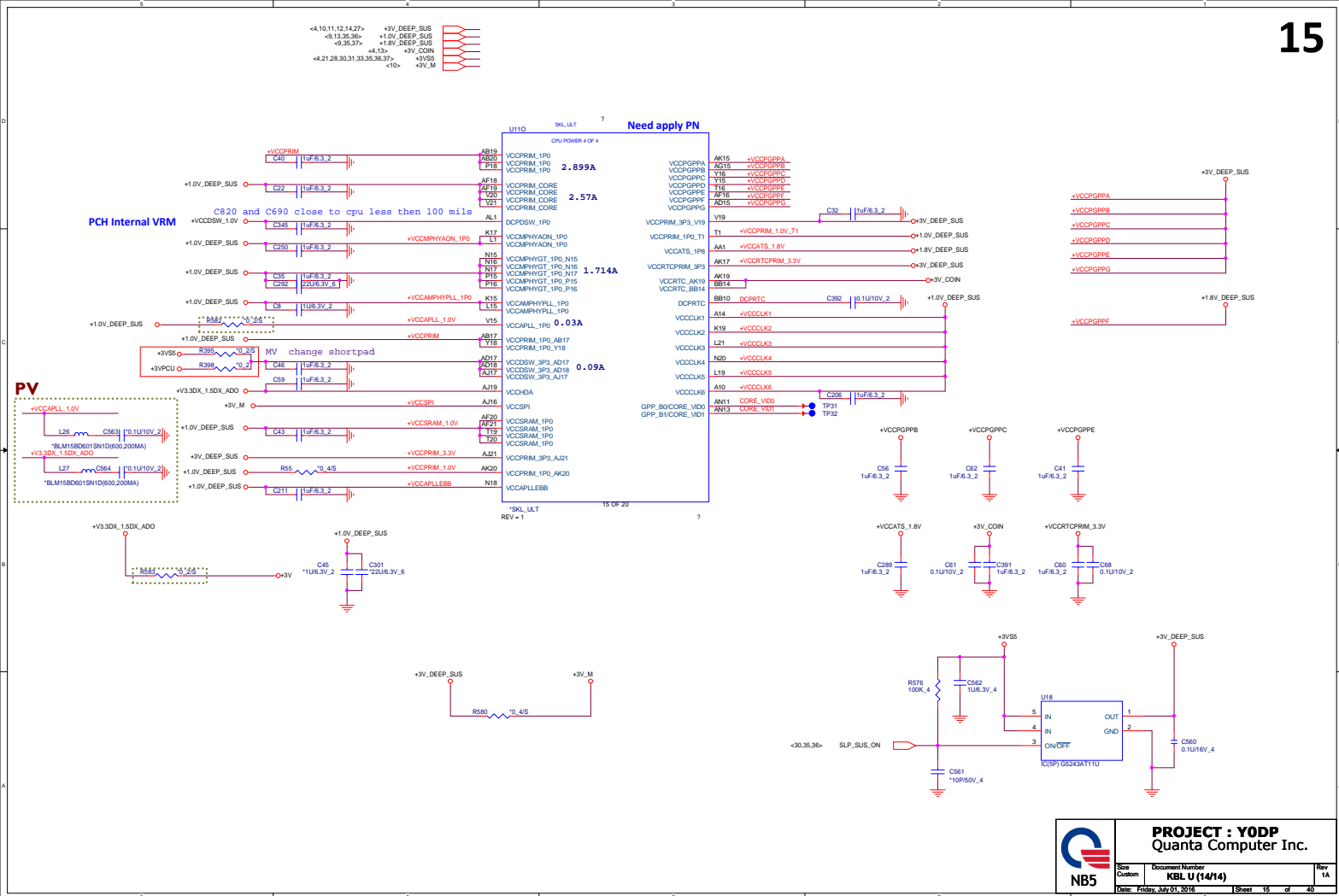


HDA Bus(CLG)

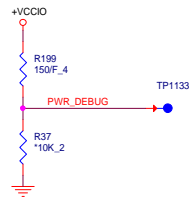


Model	BOARD_ID0	BOARD_ID7	Board ID [3:4]	BOARD_ID[3:9]
Y0DP	Reserve (Default = 0)	0:2+2 CPU 1:2+3E CPU (Default = 0)	Reserve (Default = 0)	0000:H9CCNNNCLTLAR-NUD Hynix 16GB x32bit 0001:K4EBE304EB-EGCF Samsung 16GB x32bit 0010:MT52L1G32D4PG-107 Micron 16GB x32bit 0011:MT52L12M32D2PF-107:B 8GB x32 bit 0100:H9CCNNNBJTLAR-NUD 8GB x32 bit 0101:K4E6E304EB-EGCF 8GB x32 bit (B-Die)





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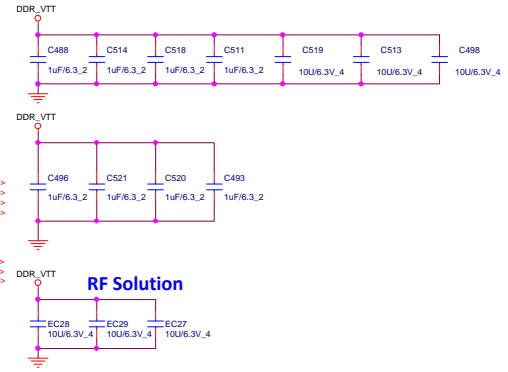
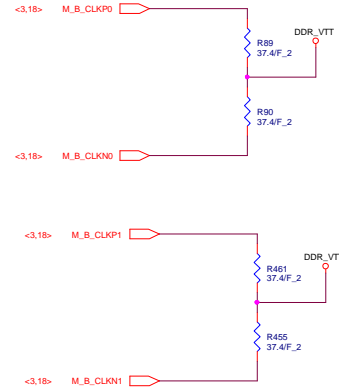
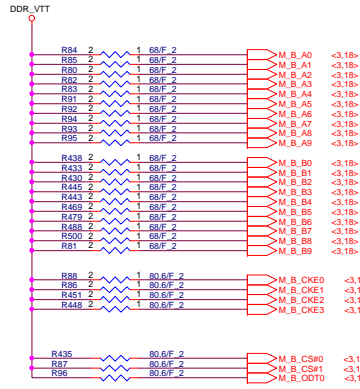
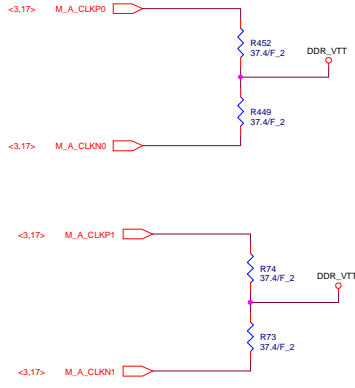
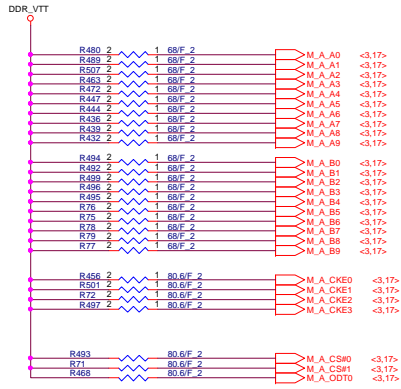


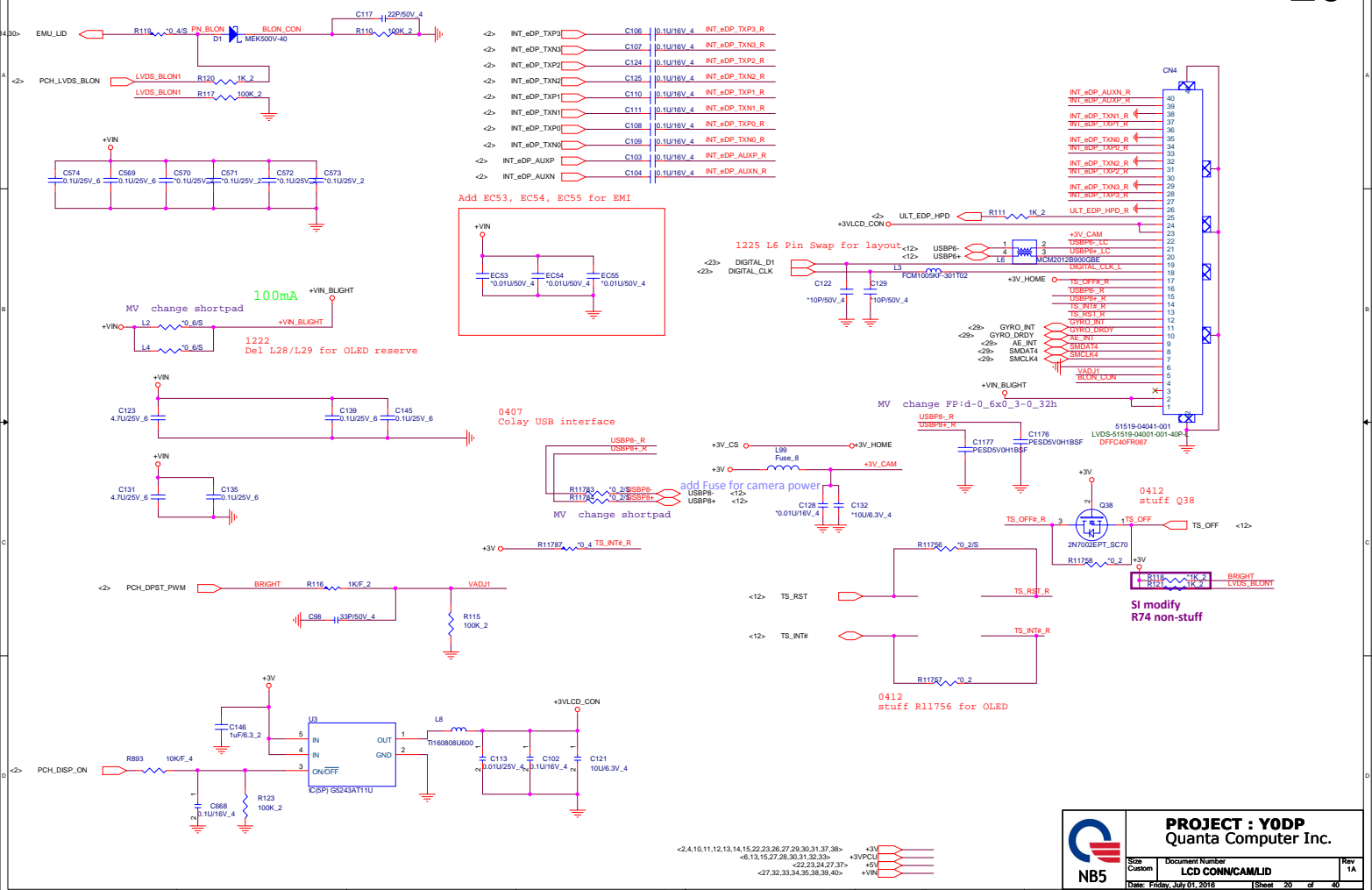
PROJECT : YODP
Quanta Computer Inc.

Size Custom	Document Number XDP/APS	Rev 1A
Date: Friday, July 01, 2016	Sheet 16 of 40	





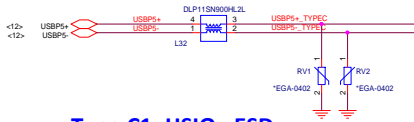




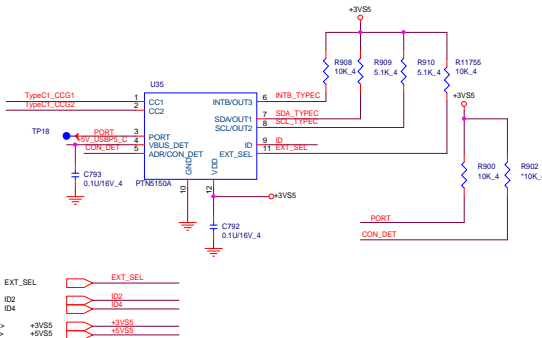
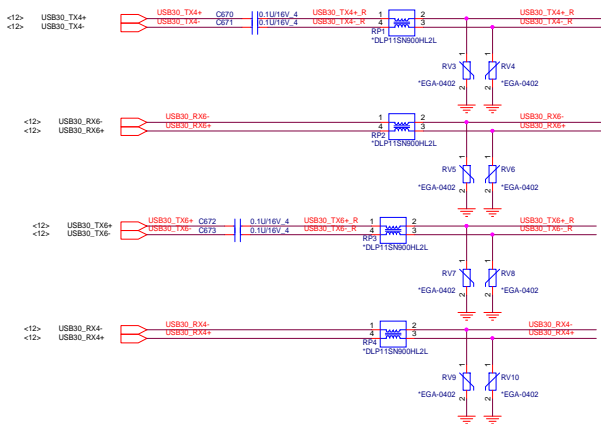
	PROJECT : YODP Quanta Computer Inc.		Rev 1A	
	Size Custom	Document Number LCD CONN/CAM/LID		Date: Friday, July 01, 2016
	Sheet 20 of 40			

USB2.0 ESD

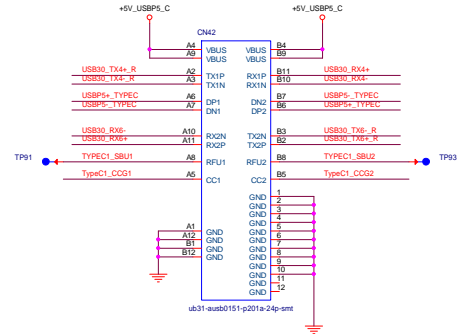
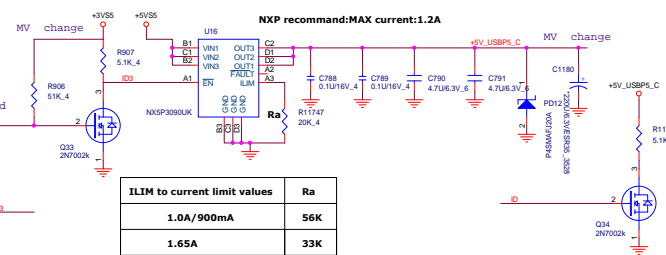
 +5V <22,23,24,27,37>
 +3V <2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38>



Type C1_HSIO_ESD




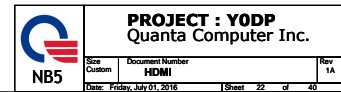
ILIM to current limit values	Ra
1.0A/900mA	56K
1.65A	33K
2.5A	20K
3.5A	14K

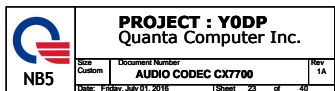


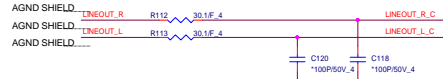
MV change FP:ub31-ausb0151-p201a-24p-smt

MV del

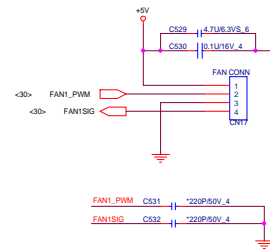
 NB5	PROJECT : YODP Quanta Computer Inc.		
	Size Custom	Document Number USB TYPEC	Rev 1A
Date: Friday, July 01, 2016		Sheet 21 of 40	



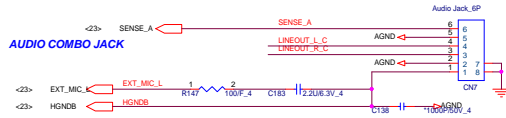





```
1203 Update footprint from 88266-0400-4p-1 to 88266-04x1-4p-1-smt
```

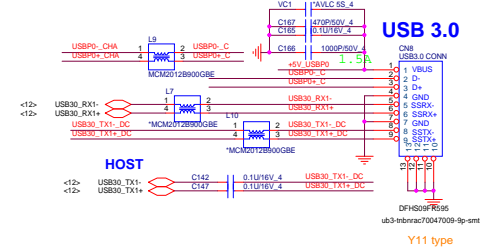
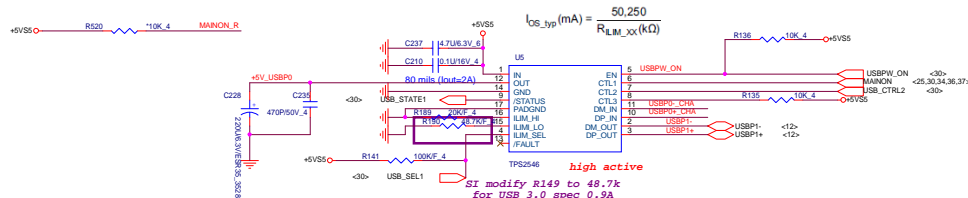


Audio Jack_6P

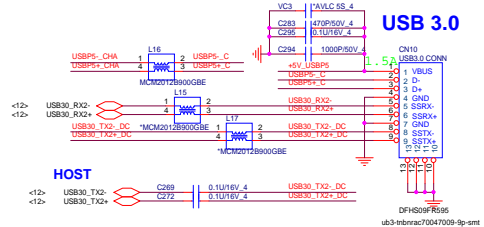
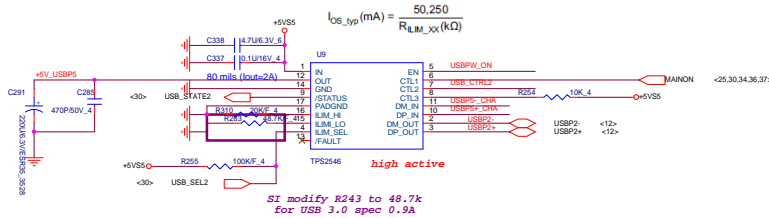


 NB5	PROJECT : YODP Quanta Computer Inc.		
	Size Custom	Document Number AUDIO AMP	Rev 1A
Date: Friday, July 01, 2016		Sheet 24 of 40	

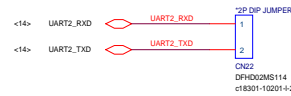
PV ADD R554/R555/R556 10k for USB 3.0 PU



1203
Update footprint from ub3-tmbnrc70047009-9p to ub3-tmbnrc70047009-9p-smt



Intel UART



Left side USB 2.0/3.0 Combo

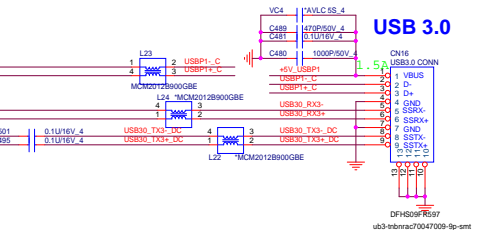
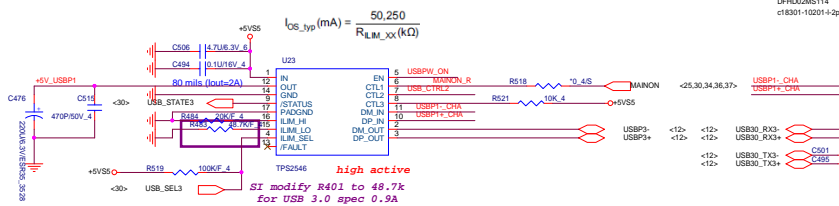


Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2546 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	0	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, load detection with ILIM_LO + 60mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

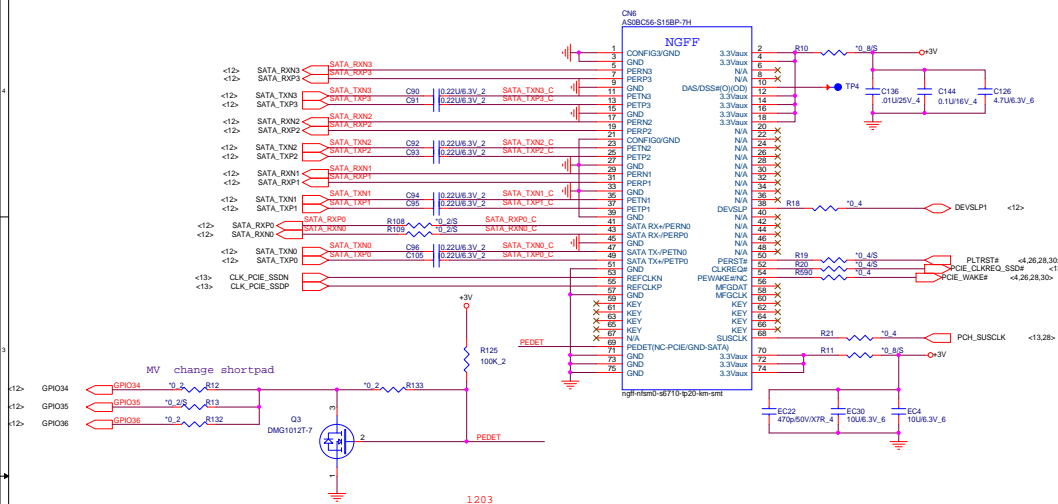
<4.15,21,28,30,31,33,35,36,37>
<4.21,33,34,35,36,37,38,39,40>
<4.13,15,27,28,30,31,32,33>

+5V USBP1
+5V USBP2
+5V USBP3



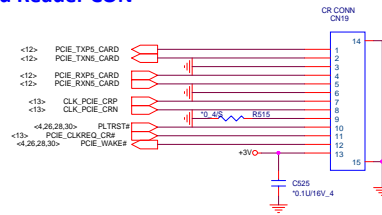
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Quanta Computer Inc.

Doc: P04px_July01_2016
Doc Number: USB20/30
Rev 1A



TPM (2.0)

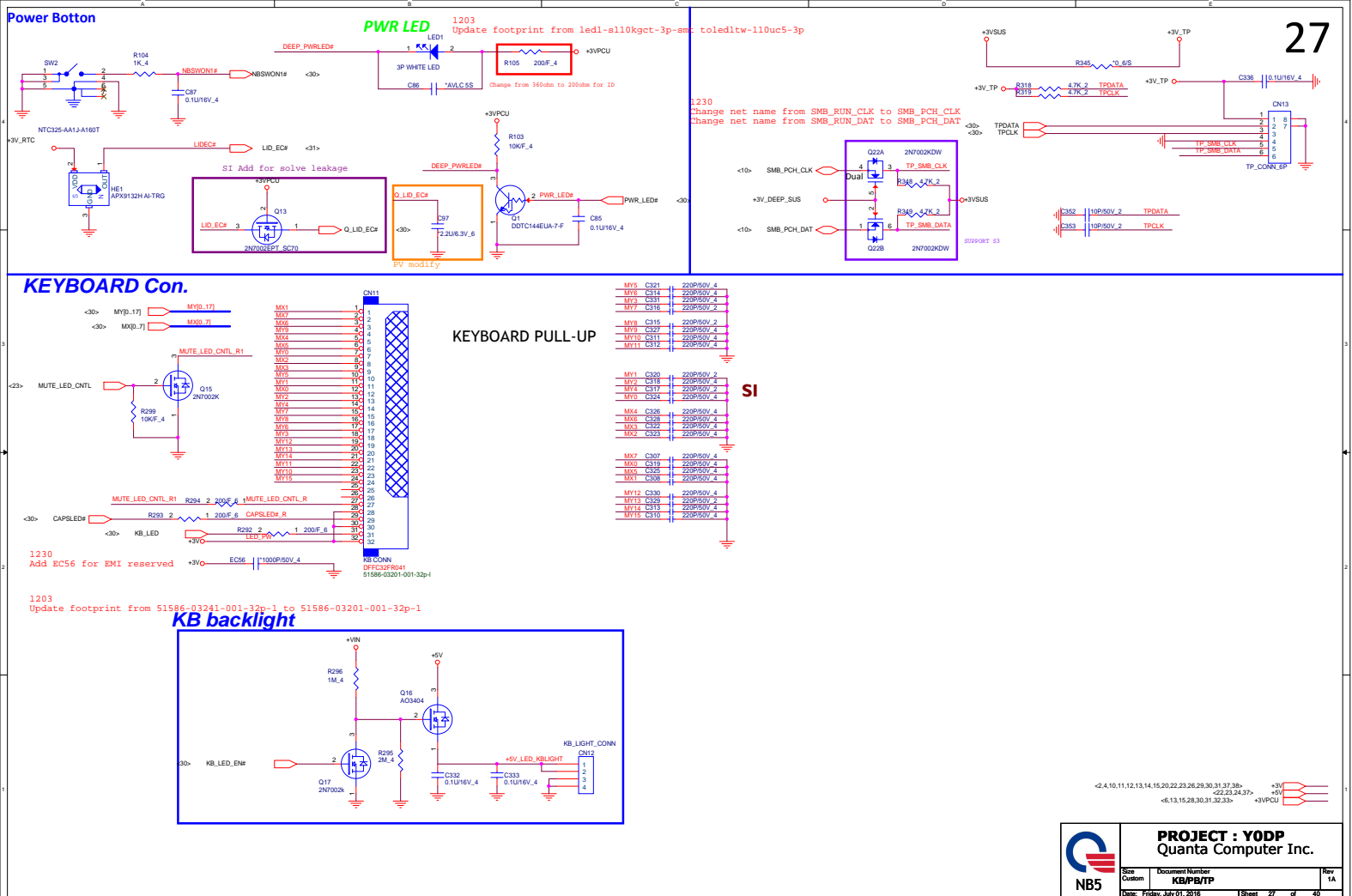
Card Reader CON



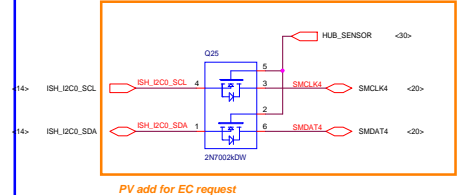
<2,4,10,11,12,13,14,15,20,22,23,27,29,30,31,37,38> +3V
<22,23,24,27,37> +5V
<6,13,15,27,28,30,31,32,33> +9VPCU


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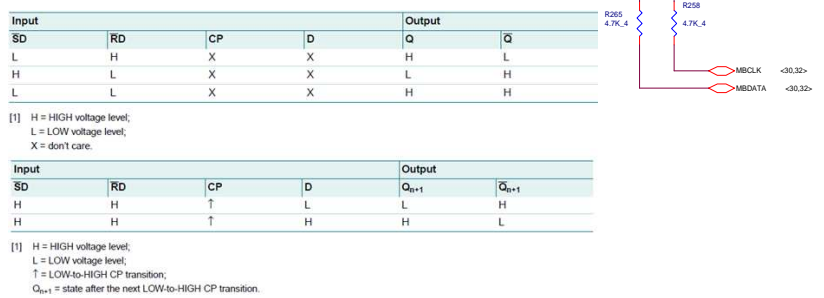
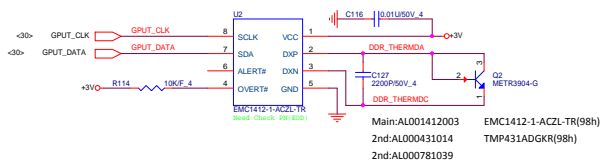
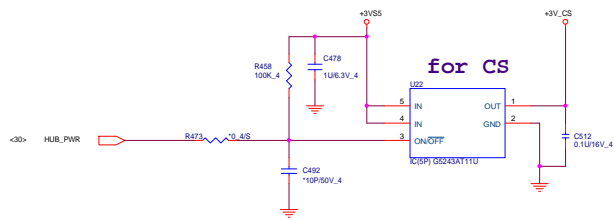
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	Size Custom	Document Number SENSOR HUB	Rev 1A
Date: Friday, July 01, 2016		Sheet 29 of 40	

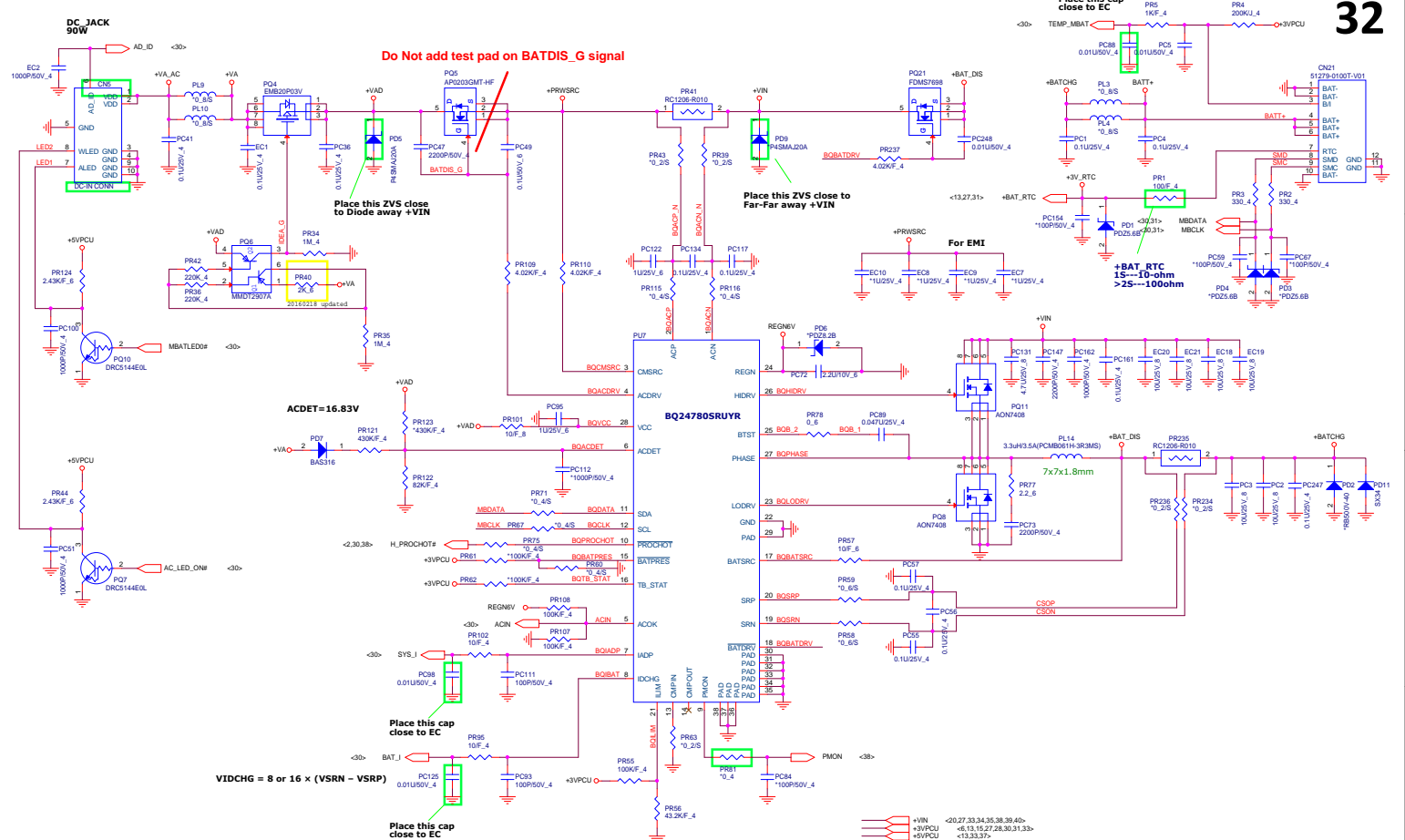


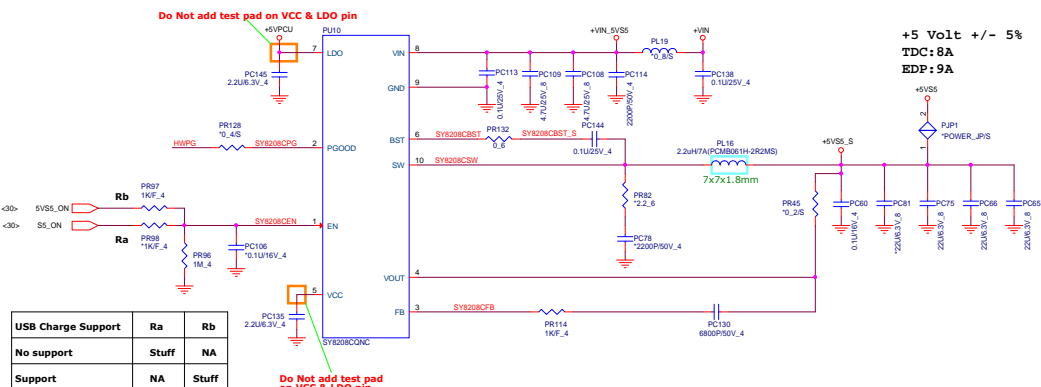
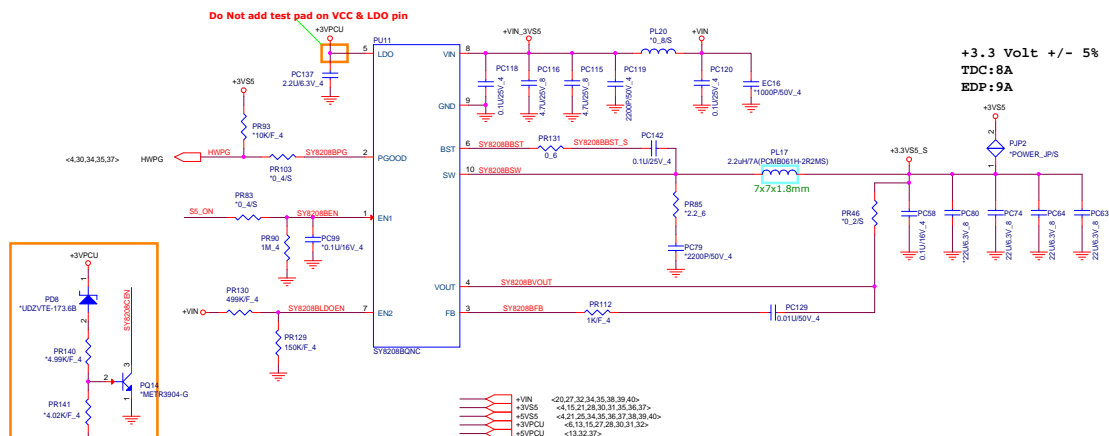
Input				Output	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

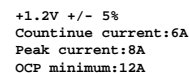
[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Input				Output	
SD	RD	CP	D	Q _{n+1}	Q̄ _{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

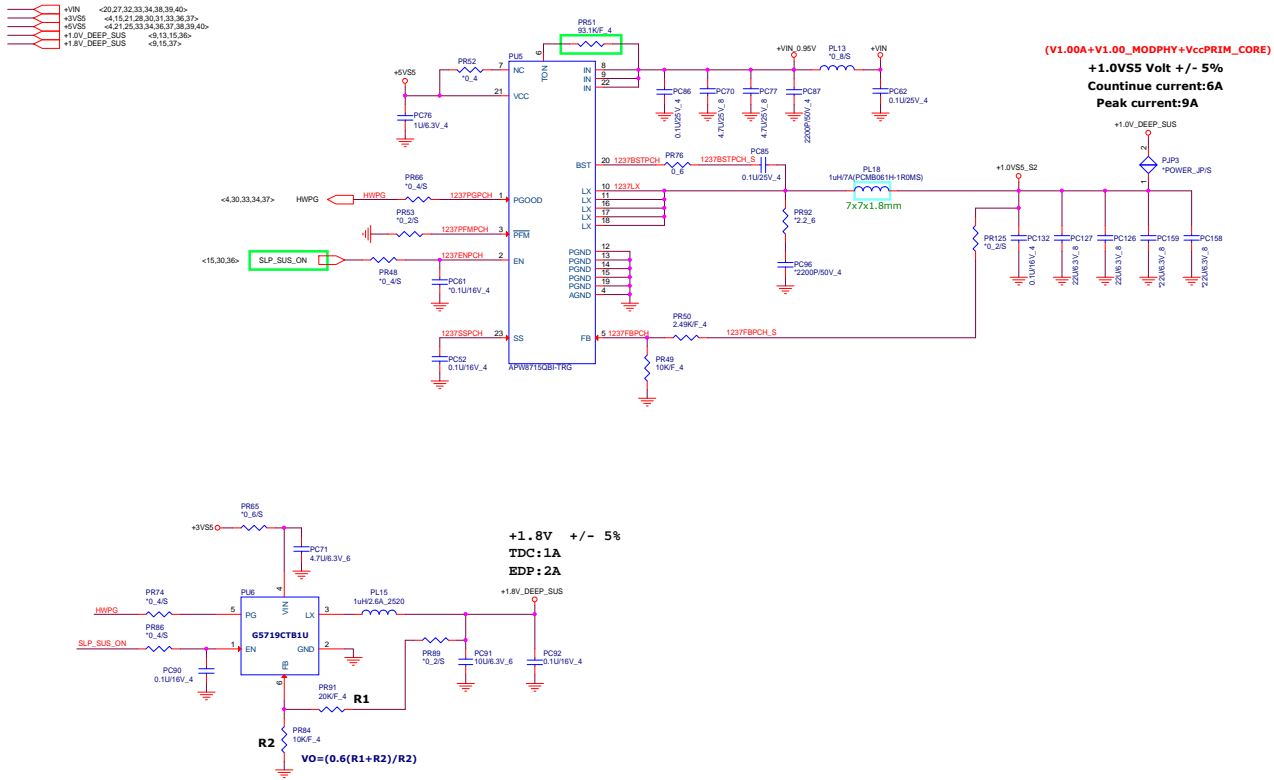
[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.






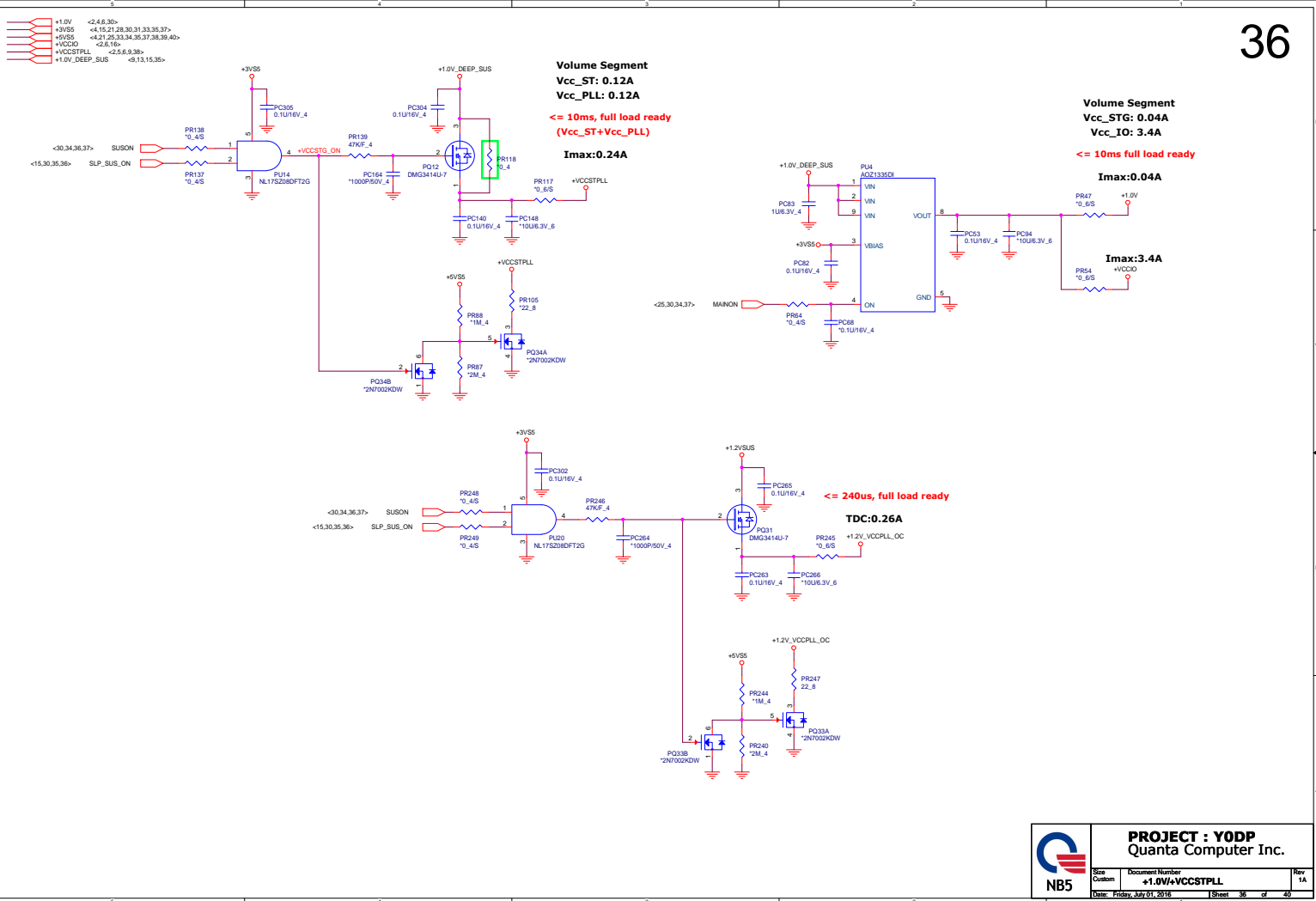


	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

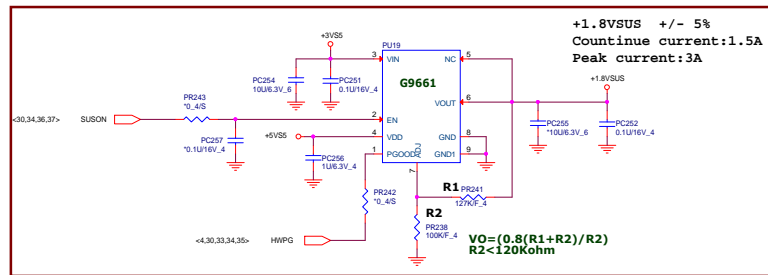
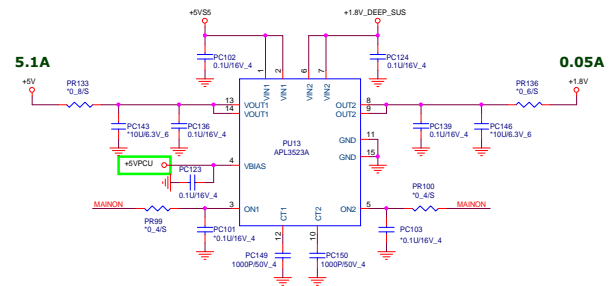
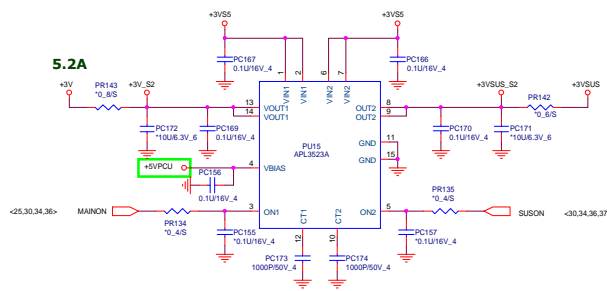


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	Set	Document Number	Rev
	Custom	+1.0V+1.5V+1.8V_DEEP_SUS	1A

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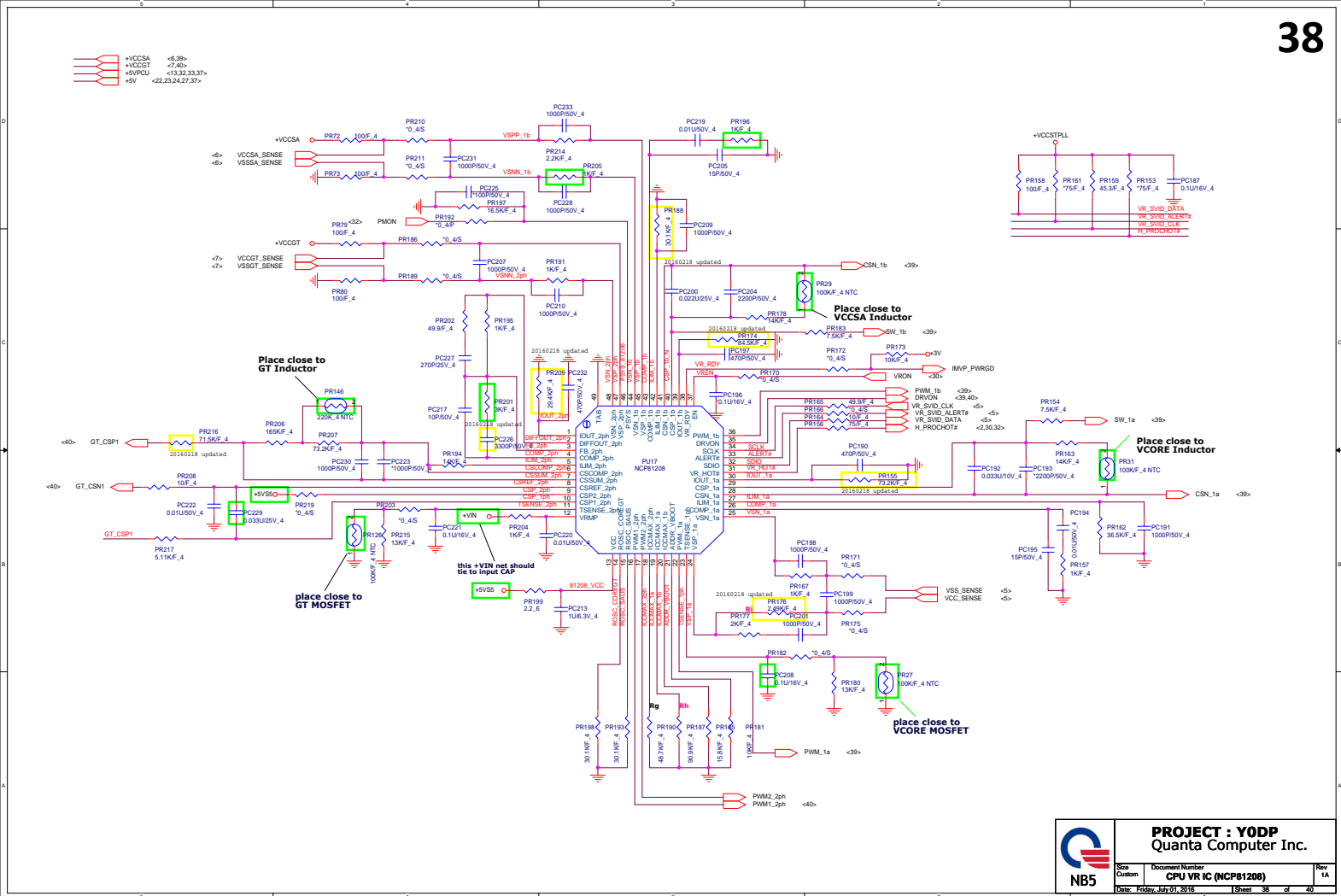


+3V	<2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,38>
+5V	<22,23,24,27,37>
+5VS	<4,15,21,28,30,31,33,35,36>
+5VS2	<4,21,28,33,34,35,36,38,39,40>
+5VSUS	<37,38>
+1.8V_DEEP_SUS	<8,15,35>
+1.8V	<25>
+5V	<22,23,24,27,37>
+VM	<20,27,32,33,34,35,38,39,40>
+1.8VSUS	<17,18>

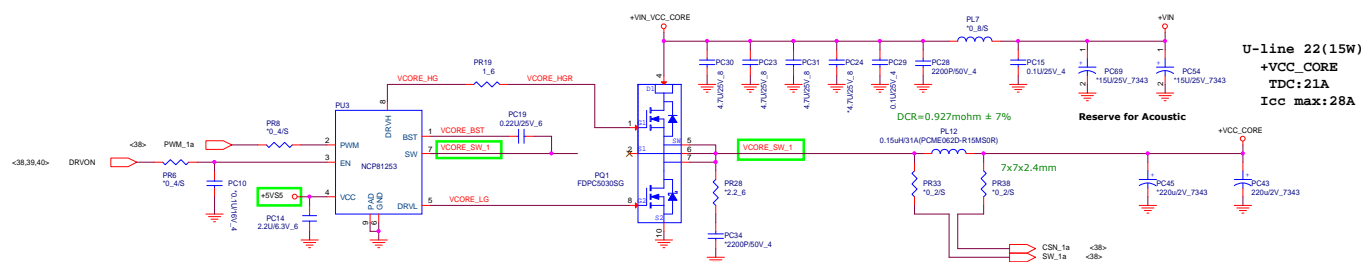


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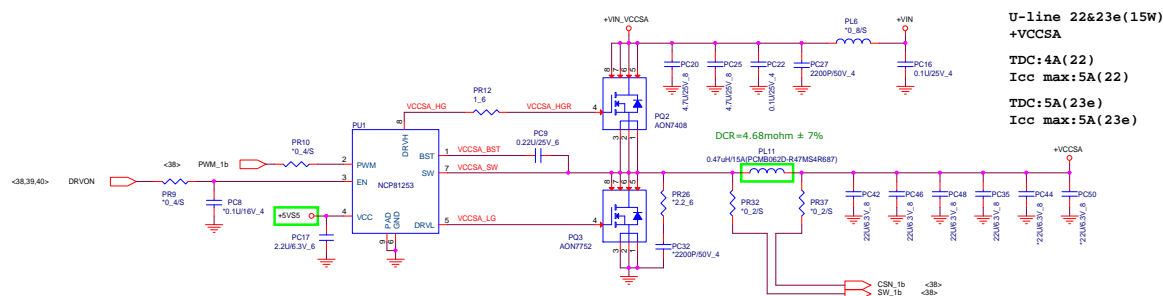
NB5	PROJECT : YODP		
	Quanta Computer Inc.		
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Custom	Load switch IC		
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VCCSA



	PROJECT : YODP Quanta Computer Inc.		
	Set Content	Document Number +VCCORE/VCCSA (NCP81253)	Rev 1A

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